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## IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with <u>underlining</u> and deleted text with <u>strikethrough</u>. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 1-47 and ADD new claim 48 in accordance with the following:

- 1. (CANCELLED)
- 2. (CANCELLED)
- 3. (CANCELLED)
- 4. (CANCELLED)
- 5. (CANCELLED)
- 6. (CANCELLED)
- 7. (CANCELLED)
- 8. (CANCELLED)
- 9. (CANCELLED)
- 10. (CANCELLED)
- 11. (CANCELLED)
- 12. (CANCELLED)
- 13. (CANCELLED)

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- 14. (CANCELLED)
- 15. (CANCELLED)
- 16. (CANCELLED)
- 17. (CANCELLED)
- 18. (CANCELLED)
- 19. (CANCELLED)
- 20. (CANCELLED)
- 21. (CANCELLED)
- 22. (CANCELLED)
- 23. (CANCELLED)
- 24. (CANCELLED)
- 25. (CANCELLED)
- 26. (CANCELLED)
- 27. (CANCELLED)
- 28. (CANCELLED)
- 29. (CANCELLED)

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- 30. (CANCELLED)
- 31. (CANCELLED)
- 32. (CANCELLED)
- 33. (CANCELLED)
- 34. (CANCELLED)
- 35. (CANCELLED)
- 36. (CANCELLED)
- 37. (CANCELLED)
- 38. (CANCELLED)
- 39. (CANCELLED)
- 40. (CANCELLED)
- 41. (CANCELLED)
- 42. (CANCELLED)
- 43. (CANCELLED)
- 44. (CANCELLED)
- 45. (CANCELLED)

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- 46. (CANCELLED)
- 47. (CANCELLED)
- 48. (NEW) A memory device, comprising:

a nonvolatile memory connected to a first memory bus, and capable of storing data through said first memory bus;

a volatile memory connected to a second memory bus, and capable of being randomaccessed through said second memory bus; and

a controller having a first internal terminal connected to said first memory bus, a second internal terminal connected to said second memory bus, and an external terminal connected to an external bus, said controller for transferring data between said nonvolatile memory and said volatile memory through said first and second internal terminals,

wherein, when the data transfer is not performed, said controller controls to access from an exterior to said volatile memory through said external terminal and said second internal terminal, in accordance with an instruction through said external bus, and

said controller performs error detection and/or correction processing in said data transfer.